REMARKS

Claims 1-9 are remain pending in this application. Claim 1 is independent. In light of the remarks made herein, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections.

In the outstanding Official Action, the Examiner rejected claims 1-3 and 6 under 35 U.S.C. § 103(a) as being unpatentable over *Furuhashi et al.* (USP 5,909,205) in view of *Kinoshita et al.* (USP 5,771,031); rejected claims 4 and 5 under 35 U.S.C. § 103(a) as being unpatentable over *Furuhashi et al.* in view of *Kinoshita et al.* and *Nally et al.* (USP 5,808,629); rejected claims 7 and 8 under 35 U.S.C. § 103(a) as being unpatentable over *Furuhashi et al.* and *Kinoshita et al.*, and further in view of *Tada et al.* (USP 6,252,563); and rejected claim 9 under 35 U.S.C. § 103(a) as being unpatentable over *Furuhashi et al.* and *Kinoshita et al.*, and further in view of *Selwan et al.* (USP 5,526,025). Applicants respectfully traverse these rejections.

Claim Rejections - 35 U.S.C. § 103 - *Furuhashi et al./Kinoshita et al.*

In support of the Examiner's rejection of claim 1, the Examiner admits that *Furuhashi et al.* fails to disclose a number of line memories being read out by way of specifying the address of the display data for one line and specifically, selection of a line memory from a number of line memories. The Examiner relies on the

teachings of *Kinoshita et al.* to cure the deficiencies of the teachings of *Furuhashi et al.* by asserting that *Kinoshita et al.* discloses a liquid crystal controller with a data distribution circuit with a selector WS, memories M1-M3, and a selector RS, where the selector WS selects one of the memories M1, M2, and M3. The Examiner concludes it would have been obvious to a person of ordinary skill in the art to modify *Furuhashi et al.* with the selector and plural memories as disclosed by *Kinoshita et al.*, asserting it is possible to increase the data items and the word length without increasing the storage capacity of the memories resulting in cost reduction. Applicants respectfully disagree with the Examiner's assertions that *Kinoshita et al.* cures the deficiencies of the teachings of *Furuhashi et al.*

The disclosure of *Kinoshita et al.* is directed to a flat-panel display device and driving method. Specifically, at col. 8, lines 42-50, *Kinoshita et al.* discloses as follows:

> ...the selector WS selects memories M1, M2, and M3 in this order, and supplies RGB pixel data SD sequentially supplied from outside to the selected one of the memories M1, M2, and M3. The write control signals WM1, WM2, and WM3 are sequentially changed each time one hundred items of RGB pixel data SD are supplied. The selected memory stores the RGB pixel data SD supplied from the selector WS into a write memory area designated by a write address signal WADRS.

In contrast, the present invention as set forth in claim 1 recites, *inter alia*, a programmable display device wherein the

display control section reads out the display data by specifying the address of the display data for one line which has a possibility to be displayed on the screen to the main memory from which the display data is transferred, based on the stored information, causing the data processing circuit to perform the data transfer and select the line memory to store the display data.

As can be seen from the above, *Kinoshita et al.* discloses RGB pixel data is sequentially supplied from outside to the selected one of the memories. There is no teaching or suggestion in *Kinoshita et al.* that is directed to the display control section reading out the display data by specifying the address of the display data for one line which has a possibility to be displayed on the screen to the main memory from which the display data is transferred.

It appears, based upon the Examiner's statements in the outstanding Official Action, that the Examiner is confusing the reading function of the display control section. The Examiner recites that *Furuhashi et al.* fails to disclose a number of line memories being read out by way of specifying the address of the display data for one line. However, this element is not recited in the claim. The claim recites a display control section reading out the display data by specifying the address of the display data for one line which has the possibility to be displayed on the screen to the main memory from which the display data is transferred, based

on the stored information, causing the data processing circuit to perform the data transfer and select the line memory to store the display data. As such, the line memories are not read out by way of specifying the address of the display data for one line as asserted by the Examiner.

As *Kinoshita et al.* fails to cure the deficiencies of the teachings of *Furuhashi et al.*, neither of the references, either alone or in combination, teach or suggest all of the claim elements (assuming these references are combinable, which Applicants do not admit). As the Examiner has failed to provide references that teach or suggest all of the claim elements, it is respectfully submitted that the Examiner has failed to establish *prima facie* obviousness under 35 U.S.C. § 103. It is respectfully requested that the outstanding rejection be withdrawn.

It is respectfully submitted that claims 2-9 are allowable for the reasons set forth above with regard to claim 1 at least based upon their dependency on claim 1.

Conclusion

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Catherine M. Voisinet (Reg. No. 52,327) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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